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EXAMINER	
IWASHKO, LEV	
ART UNIT	**PAPER NUMBER**
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,632	ADELMANN ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/17/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 5-6, 10-15, and 17-20 are rejected under U.S.C. 102(b) as being anticipated by Davis et al. (US Patent 5,717,648).

Claim 1. An integrated circuit device that comprises: *(Column 3, line 67 – Discloses an integrated circuit chip)*

- a memory array integrated on a substrate, *(Column 15, lines 1-2 – Claim that the memory array is on an integrated circuit substrate)*
- wherein the memory array stores data in encoded form; *(Column 12, lines 45-49 – State the following: "Each of these storage areas store a two big signal corresponding to one of the cache lines. These 2 bits are the encoded equivalent of the HITA-D lines which are encoded by encoder ENC of FIG. 3 and are only valid when a HIT occurs")*
- a decoder integrated on said substrate, coupled to the memory array and configured to decode data retrieved from the memory array; *(Column 7, lines 56-67 – State the following: "FIG. 4 is a circuit diagram of a portion of the array 41 of the integrated cache 40 of the invention. The array includes a plurality of master word lines MWL0 through MWL255 (for ease of illustration, only the first master word line MWL0 and last master word line MWL255 are shown, the remainder being generally indicated by the dotting in the middle of the Figure. In practice, the cache would include at least four redundant master word lines, and a dummy word line for timing purposes). The*

received index address A.sub.11 -A.sub.4 will be decoded by the master word line decoders MWL0 DECODE through MWL255 DECODE to determine which of the 256 master word lines are to be enabled")

- and a cache integrated on said substrate, *(Column 6, lines 6-11 – State the following: "In both embodiments, the cache 40 is integrated with the other circuitry on the microprocessor 10. By having these circuit blocks on the same chip, process sensitivities and other performance detractors resulting from these structures being formed on different chips using different processing techniques, etc. are minimized")*
- wherein the cache is configured to retrieve data stored in the memory array in anticipation of a request for said data. *(Column 1, lines 23-32 – State the following: "In order to address this problem, cache memory has been used to store data for processor operations. Typically, data is downloaded from the DRAM main memory to the cache. The cache is typically made up of an array of static RAM cells (SRAMs can be accessed at rates far faster than those of DRAMs--current state of the art SRAMs can produce data rates on the order of 5 nanoseconds). There are a number of known branch prediction or initial cache loading algorithms that determine how the cache is to be initially loaded with data." Column 6, lines 12-27 – State the following: "An overall block diagram of the cache 40 of FIGS. 1 and 2 is shown in FIG. 3. The cache 40 includes a storage array 41. The array includes a DATA portion that stores four cache lines A-D, a TAG portion that stores tags A-D corresponding to the four cache lines, an LRUA portion that stores the least recently used information in storage areas MRU1, MRU2, MRU3, and LRU, and a valid portion that stores the data valid information for each cache line A-D. A feature of the invention is that all of this data for a single set is stored on a single, physically addressable word line. Thus, as will be*

discussed in more detail below, a single word line is coupled to memory cells in each of the above-mentioned arrays, such that by accessing a single physically addressable word line all of the aforementioned data can be accessed")

Claim 2. The device of claim 1, wherein the decoder is coupled between the memory array and the cache, and wherein the cache stores decoded data. *(Column 7, lines 56-67 – State the following: "FIG. 4 is a circuit diagram of a portion of the array 41 of the integrated cache 40 of the invention. The array includes a plurality of master word lines MWL0 through MWL255 (for ease of illustration, only the first master word line MWL0 and last master word line MWL255 are shown, the remainder being generally indicated by the dotting in the middle of the Figure. In practice, the cache would include at least four redundant master word lines, and a dummy word line for timing purposes). The received index address A.sub.11 -A.sub.4 will be decoded by the master word line decoders MWL0 DECODE through MWL255 DECODE to determine which of the 256 master word lines are to be enabled")*

Claim 3. The device of claim 1, wherein the cache is coupled between the memory array and the decoder, and wherein the cache stores encoded data. *(Column 12, lines 45-49 – State the following: "Each of these storage areas store a two big signal corresponding to one of the cache lines. These 2 bits are the encoded equivalent of the HITA-D lines which are encoded by encoder ENC of FIG. 3 and are only valid when a HIT occurs")*

Claim 5. The device of claim 1, further comprising:

- a selection circuit coupled to the memory array to select a set of one or more memory cells in response to an address value; *(Column 10, lines 44-46 – State the following: "In operation, one of the master word lines MWL0 . . . MWL255 are selected and driven as a function of the index address on the master word line decoders")*

- and a sense circuit coupled to the memory array to sense data stored in the selected set of memory cells, wherein the cache is configured to receive a read operation comprising an address value, and is further configured to provide the address value to the selection circuit if the cache does not have a copy of data stored in the corresponding set of memory cells. *(Column 10, lines 46-65 – State the following: "As one of the master word lines are selected to select a given set, the information in the TAG, LRU, and VALID arrays for each of the cache lines A-D is accessed and sensed. As shown in FIG. 11B, a CMOS sense amplifier with conventional cross coupled inverter pairs is used, having p-type bit line isolation devices ISO1, ISO2 receiving as their control input the SASET signal, to isolate the bit lines from the sense amp cross coupled pair during sensing. This feature is needed to accommodate the Read-Modify-Write cycle of the LRU, TAG and Valid arrays. This sense amp is also a power reduction feature in that the bit lines are not driven throughout the cycle, thus they are never fully discharged except during a write cycle. As discussed above in conjunction with FIG. 3, if the accessed tag does not agree with the tag received from the processor, none of the cache lines A-D at the accessed set is storing the requested information and access to the cache lines is terminated by disabling the read/write enable block 160 by receipt of the MISS signal from XOR 140")*

Claim 6. The device of claim 5, further comprising: wherein the cache is further configured to determine a set of one or more predicted address values and to provide the set of predicted address values to the selection circuit. *(Column 1, lines 23-32 – State the following: "In order to address this problem, cache memory has been used to store data for processor operations. Typically, data is downloaded from the DRAM main memory to the cache. The cache is typically made up of an array of static RAM cells (SRAMs can be accessed at rates far faster than those of DRAMs--*

current state of the art SRAMs can produce data rates on the order of 5 nanoseconds). There are a number of known branch prediction or initial cache loading algorithms that determine how the cache is to be initially loaded with data." Column 6, lines 12-27 – State the following: "An overall block diagram of the cache 40 of FIGS. 1 and 2 is shown in FIG. 3. The cache 40 includes a storage array 41. The array includes a DATA portion that stores four cache lines A-D, a TAG portion that stores tags A-D corresponding to the four cache lines, an LRUA portion that stores the least recently used information in storage areas MRU1, MRU2, MRU3, and LRU, and a valid portion that stores the data valid information for each cache line A-D. A feature of the invention is that all of this data for a single set is stored on a single, physically addressable word line. Thus, as will be discussed in more detail below, a single word line is coupled to memory cells in each of the above-mentioned arrays, such that by accessing a single physically addressable word line all of the aforementioned data can be accessed". Column 4, lines 35-41- State the following: "In yet another aspect, the present invention comprises a central processor unit, a main memory for storing data, and a cache unit having a plurality of index lines, each of said index lines storing a plurality of data words from selected locations in said main memory, a method of writing an update data word from said main memory to said cache")

Claim 10. A method of providing access to stored data, the method comprising:

- receiving an address value at a cache *(Column 12, lines 21-26 – State the following: "The access to the designated tag is continued as discussed above. If this signal indicates a cache MISS during a write cycle, the CPU must go to main memory for the data, and will store the data in the cache at the given index address at the cache line designated by the LRU CONTROL 150")*

- integrated on a substrate; *(Column 6, lines 6-11 – State the following: "In both embodiments, the cache 40 is integrated with the other circuitry on the microprocessor 10. By having these circuit blocks on the same chip, process sensitivities and other performance detractors resulting from these structures being formed on different chips using different processing techniques, etc. are minimized")*
- retrieving encoded data associated with the address value from a memory cell array integrated on said substrate if the cache does not possess data associated with the address value; *(Column 12, lines 41-49 – State the following: "Then, if another cache MISS occurs for that given set, the LRU portion of the cycle is invoked. As shown in FIG. 3, the LRUA array in the cache is organized into four storage areas MRU1, MRU2, MRU3, and LRU. Each of these storage areas store a two big signal corresponding to one of the cache lines. These 2 bits are the encoded equivalent of the HITA-D lines which are encoded by encoder ENC of FIG. 3 and are only valid when a HIT occurs")*
- decoding the encoded data; *(Column 12, lines 46-61 – State the following: "These 2 bits are the encoded equivalent of the HITA-D lines which are encoded by encoder ENC of FIG. 3 and are only valid when a HIT occurs. The MRU1 storage area stores a two-bit signal for the cache line A-D that was most recently used; the MRU2 storage area stores a two-bit signal for the cache line A-D that was next most recently used; the MRU3 storage area stores a two-bit signal for the cache line A-D that was next most recently used; and the LRU storage array stores a two-bit signal for the cache line A-D that was least recently used. Thus, in the LRU mode the portion A-D indicated by the LRU storage area will be accessed. The LRU CONTROL 150 simply outputs the two-bit signal stored by the LRU storage area, decodes it to 4 hit signals and sends it to the LWL CONTROL 200, and*

the section select and sense amp enable signals for that portion will be output")

- and providing decoded data as a response to receiving said address value. *(Column 10, lines 44-46 – State the following: "In operation, one of the master word lines MWL0 . . . MWL255 are selected and driven as a function of the index address on the master word line decoders")*

Claim 11. The method of claim 10, wherein said retrieving comprises: retrieving encoded data associated with a block of address values containing the received address value if the cache does not possess data associated with the received address value. *(Column 12, lines 41-49 – State the following: "Then, if another cache MISS occurs for that given set, the LRU portion of the cycle is invoked. As shown in FIG. 3, the LRUA array in the cache is organized into four storage areas MRU1, MRU2, MRU3, and LRU. Each of these storage areas store a two big signal corresponding to one of the cache lines. These 2 bits are the encoded equivalent of the HITA-D lines which are encoded by encoder ENC of FIG. 3 and are only valid when a HIT occurs")*

Claim 12. The method of claim 11, wherein said retrieving further comprises: storing the retrieved encoded data in the cache. *(Column 12, lines 45-49 – State the following: "Each of these storage areas store a two big signal corresponding to one of the cache lines. These 2 bits are the encoded equivalent of the HITA-D lines which are encoded by encoder ENC of FIG. 3 and are only valid when a HIT occurs")*

Claim 13. The method of claim 11, wherein said retrieving further comprises: storing decoded data in the cache. *(Column 7, lines 56-67 – State the following: "FIG. 4 is a circuit diagram of a portion of the array 41 of the integrated cache 40 of the invention. The array includes a plurality of master word lines MWL0 through MWL255 (for ease of illustration, only the first master word line MWL0 and last master word line MWL255 are shown,*

the remainder being generally indicated by the dotting in the middle of the Figure. In practice, the cache would include at least four redundant master word lines, and a dummy word line for timing purposes). The received index address A.sub.11 -A.sub.4 will be decoded by the master word line decoders MWL0 DECODE through MWL255 DECODE to determine which of the 256 master word lines are to be enabled")

Claim 14. The method of claim 10, further comprising: retrieving encoded data associated with a subsequent block of address values if the cache does not possess data associated with the subsequent block of address values. *(Column 12, lines 41-56 – State the following: "Then, if another cache MISS occurs for that given set, the LRU portion of the cycle is invoked. As shown in FIG. 3, the LRUA array in the cache is organized into four storage areas MRU1, MRU2, MRU3, and LRU. Each of these storage areas store a two big signal corresponding to one of the cache lines. These 2 bits are the encoded equivalent of the HITA-D lines which are encoded by encoder ENC of FIG. 3 and are only valid when a HIT occurs. The MRU1 storage area stores a two-bit signal for the cache line A-D that was most recently used; the MRU2 storage area stores a two-bit signal for the cache line A-D that was next most recently used; the MRU3 storage area stores a two-bit signal for the cache line A-D that was next most recently used; and the LRU storage array stores a two-bit signal for the cache line A-D that was least recently used")*

Claim 15. The method of claim 14, wherein the subsequent block of address values numerically immediately follows the block of address values containing the received address value. *(Column 12, lines 49-46 – State the following: "The MRU1 storage area stores a two-bit signal for the cache line A-D that was most recently used; the MRU2 storage area stores a two-bit signal for the cache line A-D that was next most recently used; the MRU3 storage area stores a two-bit signal for the cache line A-D that was next*

most recently used; and the LRU storage array stores a two-bit signal for the cache line A-D that was least recently used")

Claim 17. The method of claim 10, further comprising: retrieving encoded data associated with multiple subsequent blocks of address values. *(Column 12, lines 41-56 – State the following: "Then, if another cache MISS occurs for that given set, the LRU portion of the cycle is invoked. As shown in FIG. 3, the LRUA array in the cache is organized into four storage areas MRU1, MRU2, MRU3, and LRU. Each of these storage areas store a two big signal corresponding to one of the cache lines. These 2 bits are the encoded equivalent of the HITA-D lines which are encoded by encoder ENC of FIG. 3 and are only valid when a HIT occurs. The MRU1 storage area stores a two-bit signal for the cache line A-D that was most recently used; the MRU2 storage area stores a two-bit signal for the cache line A-D that was next most recently used; the MRU3 storage area stores a two-bit signal for the cache line A-D that was next most recently used; and the LRU storage array stores a two-bit signal for the cache line A-D that was least recently used")*

Claim 18. The method of claim 17, wherein at least one of said multiple subsequent blocks immediately follows in numerical order the block of address values containing the received address value, and wherein at least one of said multiple subsequent blocks statistically follows the block of address values containing the received address value. *(Column 12, lines 49-46 – State the following: "The MRU1 storage area stores a two-bit signal for the cache line A-D that was most recently used; the MRU2 storage area stores a two-bit signal for the cache line A-D that was next most recently used; the MRU3 storage area stores a two-bit signal for the cache line A-D that was next most recently used; and the LRU storage array stores a two-bit signal for the cache line A-D that was least recently used")*

Claim 19. A digital device comprising: *(Column 3, lines 10-15 – Declare computers and PDAs)*

- an assisted memory device having a cache integrated on the same substrate; *(Column 15, lines 1-2 – Claim that the memory array is on an integrated circuit substrate. Column 6, lines 6-11 – State the following: "In both embodiments, the cache 40 is integrated with the other circuitry on the microprocessor 10. By having these circuit blocks on the same chip, process sensitivities and other performance detractors resulting from these structures being formed on different chips using different processing techniques, etc. are minimized")*
- and a processor coupled to the assisted memory device and configured to operate on information stored in the assisted memory device. *(Column 1, lines 23-25 – State the following: "In order to address this problem, cache memory has been used to store data for processor operations. Typically, data is downloaded from the DRAM main memory to the cache")*

Claim 20. The device of claim 19, wherein the information comprises software instructions for execution by the processor, and wherein the information further comprises data to be operated on in accordance with the software instructions. *(Column 5, lines 50-53 – State the following: "In general, the microprocessor operates by fetching instructions from the main memory 52 through the bus 50 and the bus unit 24, or by fetching instructions from the cache through bus unit 24")*

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 4 is rejected under 35 U.S.C.103(a) as being unpatentable over Davis et al. as applied to claim 1 above, further in view of Edwards et al. (US Patent 6,628,598).

Davis teaches the limitations of claim 1 for the reasons above.

Davis' invention differs from the claimed invention in that there is no specific reference to error detection codes, error correction codes, and encryption codes.

Davis fails to teach claim 4, which states: "The device of claim 1, wherein the encoded form is in a set consisting of error detection codes, error correction codes, and encryption codes." However, Edwards claims "encoding information for any purpose, such As error detection/correction codes, Gray codes, servo bursts, and the like; product identification data such as manufacturing information, authentication information, encryption codes or keys (public or private)" (Column 7, lines 52-56). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Fully Integrated Cache Architecture" of Davis and Edwards' "Patterned Media System" before him at the time the invention was made, to combine the inventions to include error detection codes, error correction codes, and encryption codes in order to preserve data accuracy and security.

5. Claims 7-9 and 22 are rejected under 35 U.S.C.103(a) as being unpatentable over Davis et al. as applied to claims 1 and 19 above, further in view of Tran (US Patent 6,163,477) and Biggers (US Patent 4,099,266).

Davis teaches the limitations of claims 1 and 19 for the reasons above.

Davis' invention differs from the claimed invention in that there is no specific reference to two different storage technologies, namely magnetic and bi-stable.

Davis fails to teach claims 7-9 and 22, which respectively state the following: "The device of claim 1, wherein the memory array comprises memory cells of a first information storage technology, and wherein the cache comprises memory cells of a second, different information storage technology", "The device of claim 7, wherein memory cells of the first information storage technology orient magnetic fields to store information", "The device of claim 8, wherein memory cells of the second information storage technology employ bi-stable circuits to store information", and "The device of claim 19, wherein the cache comprises a memory cells of a different memory technology than a primary memory cell array of the integrated memory device." However, Tran states the following: "A typical MRAM device includes an array of memory cells. Word lines extend along rows of the memory cells, and bit lines extend along columns of the memory cells. Each memory cell is located at a cross point of a word line and a bit line. A memory cell stores a bit of information as an orientation of a magnetization. The magnetization orientation of each memory cell assumes one of two stable orientations at any given time. These two stable orientations, parallel and anti-parallel, represent logic values of "1" and "0." The magnetization orientation of a selected memory cell may be changed by supplying currents to a word line and a bit line crossing the selected memory cell. The currents create two orthogonal magnetic fields that, when combined, switch the magnetization orientation of a selected memory cell from parallel to anti-parallel or vice versa" (Column 1, lines 19-34). Biggers also states "In semiconductor MOS, memory cells are either static or dynamic. The static type of cell generally includes bi-stable circuits such as flip-flops which once set in a particular state remain in that state without periodic re-energization or "refreshing". But, static circuits require a relatively large number of devices, for example,

several field effect transistors are required to make a flip-flop. By comparison the dynamic memory cells typically employ capacitor storage and thus require fewer devices to store a bit of information, but since such storage is transient, refreshing of the information stored on the inherent capacitance is required periodically." (Column 1, lines 43-55). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Fully Integrated Cache Architecture" of Davis, the "MRAM Device" of Tran, and Biggers' "Single-Chip Bi-Polar Sense Amplifier" before him at the time the invention was made, to combine the inventions so that there would be two different types of storage technologies (one with magnetic fields and one with bi-stable circuits), so that a more diverse memory system would be included for faster access and better storage options.

6. Claims 16 and 21 are rejected under 35 U.S.C.103(a) as being unpatentable over Davis et al. as applied to claims 10, 14, and 19 above, further in view of Baker et al. (US Patent 6,266,700).

Davis teaches the limitations of claims 10, 14, and 19 for the reasons above.

Davis' invention differs from the claimed invention in that there is no specific reference to a statistics-gathering field.

Davis fails to teach claims 16 and 21, which respectively state: "The method of claim 14, wherein the subsequent block of address values statistically follows the block of address values containing the received address value, and wherein the method further comprises: maintaining for each block of address values a corresponding statistics-gathering field to predict for each block a subsequent block of address values", and "The device of claim 19, wherein the cache maintains statistics-gathering fields associated with blocks of addresses in a memory cell array

of the integrated memory device, and wherein the cache employs the fields to anticipate subsequent memory accesses by the processor." However, Baker states the following: "It is yet another object of the present invention to provide an improved system for network analysis wherein the system may determine if a particular network frame includes a protocol field that satisfies a particular statistics gathering criteria defined in a programmably configurable protocol description" (Column 4, lines 39-44). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Fully Integrated Cache Architecture" of Davis and Baker's "Network Filtering System" before him at the time the invention was made, to combine the inventions to include a include a statistics-gathering field for block prediction so that the memory system would run more quickly and efficiently.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

MATTHEW D. ANDERSON
PRIMARY EXAMINER